THE INSTITUTE OF ELECTRONICS,
INFORMATION AND COMMUNICATION ENGINEERS

IEICE ICDV 2012

A Hardware Architecture for Intra Prediction In H.264/AVC Encoder

Duy-Hieu Bui, Van-Huan Tran, Van-Mien Nguyen, Xuan-Tu Tran

SIS Laboratory, University of Engineering and Technology, Vietnam National University, Hanoi

No. 144, Xuan Thuy Road, Hanoi, 1000, Vietnam

E-mail: {hieubd, tutx, miennv, huantv}@vnu.edu.vn

Abstract MPEG-4 AVC, so called H.264/AVC, is the latest video compression standard focusing on network transport and storage of digital multimedia. This video compression technique now is widely used in satellite and cable TV, streaming internet sources for example YouTube or iTune Store, real-time videoconferencing, Blue-ray Discs and so on. However, to gain high compression ratio, H.264 encoder and decoder need a large number of computations. As a result, it is difficult to meet the real-time constraints and it also increases the power consumption which is a critical factor in embedded system and hand-held devices such as mobile phone. In H.264 system, the intra prediction module is one of the most essential parts and it is different from the previous video compression standards. With the new prediction technique, intra prediction in H.264 improves the bit rate but it also increases the memory bandwidth and the computational complexity with many prediction modes. In this work, the intra prediction procedure is fully analyzed. Based on the analysis, a hardware architecture for intra prediction focused on main profile of H.264/AVC is proposed. The proposed architecture uses an adder tree to generate the predicted pixels for all prediction modes. The cost calculation method is Sum of Absolute Transformed Difference (SATD) and mode decision is the full search scheme. The proposed architecture can do intra prediction of an HDTV input in real-time and it is successfully simulated using Modelsim and synthesized using Xilinx ISE 10.1.

Keyword H.264/AVC, Video compression, Intra prediction