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# Preface

**Welcome to the 2nd Integrated Circuits and Devices in Vietnam (ICDV2011)**

It is a great pleasure to welcome you to the ICDV 2011, the 2011 International Conference on Integrated Circuits and Devices in Vietnam. IEICE ICD has more than 10 events in a year inside Japan. The ICDV was established last year as the only international forum outside Japan to discuss leading edge research and development subjects of the integrated circuit and device field, which has served as a vehicle for a variety of exchanges and interactions among researchers and engineers, industry and academia, international communities for the future of LSI and related fields.

This year we have total of 37 oral presentations with five keynote, five invited presentations and a special talk from TJMW ("Thai-Japan MicroWave"). It is a good mix of digital, analog, and RF circuits including low power and voltage techniques, advanced VLSI designs, and their applications for image processing, wireless communications and so on. Even though ICDV may not have enough capacity today to discuss all of those issues, it will certainly contribute to create seeds for discussing new research ideas as well as help forming network among researchers, students and faculty members from a variety of institutions.

On behalf of the ICDV committee, we hope the ICDV 2011 will give Vietnamese people some opportunities to promote research and development of integrated circuit and device field.


**Masahiko Yoshimoto**
Chair of Committee on Integrated Circuits and Devices (ICD)
Professor of Kobe University,
Japan

**Ngoc-Binh Nguyen**
Rector, Professor of
University of Engineering and Technology (UET), VNU,
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# Network-on-Chips: Design and Test Challenges in Nanoscale Era

Xuan-Tu Tran

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**Abstract** — Nowadays, more and more complex intellectual property (IP) cores communicating with each other has been intently integrated into a system to meet the high demand of new applications. This make the on-chip communication become a critical issue and the conventional bus based communication using a single bus or a hierarchy of busses could not response to the communication requirements between the integrated IP cores because of their poor scalability with system size, their shared bandwidth between all the integrated IPs, and the energy efficiency requirements of final products.

To overcome those problems, the Network-on-Chip (NoC) paradigm has been proposed as a promising on-chip communication solution for designing complex systems, especially when the semiconductor technology turns into nanoscale era. However, the development of design and test methodologies for this new paradigm is a complicated and time consuming engineering process, concerning to not only hardware design issues but also network protocols matters. After a decade of research and development, the NoC designers still have to face many challenges to bring the paradigm to final industrial products.

This talk will first give a brief introduction to the network-on-chip concept, and then addresses on main challenges in designing and testing the on-chip communication network well as the attached IP cores. A practical example of designing and testing a network on chip will be also presented to illustrate the mentioned challenges.

**Keyword**: Network-on-Chip (NoC), On-chip communication, design and test challenges, testability.

## Biography

Dr. Xuan-Tu Tran was born in Nghe An, Vietnam, in 1977. He received a Bachelor of Science (B.Sc.) degree in 1999 from Hanoi University of Science and a Master of Science (M.Sc.) degree in 2003 from Vietnam National University, Hanoi, all in Electronics Engineering and Communications; and a Ph.D. degree in 2008 from the CEA-LETI, MINATEC (in collaboration with Grenoble INP), France in Micro Nano Electronics.

Xuan-Tu Tran has worked as a lecturer at Vietnam National University, Hanoi (1999-2003), as a research engineer at the CEA-LETI, MINATEC, France (2003-2008), and then as an assistant professor at the University of Engineering and Technology (UET), Vietnam National University, Hanoi (VNU) from 2008 to recent. He was a visiting/an invited professor at the University Paris-Sud 11, France (2009, 2010), a visiting professor at Grenoble INP in 2011. He is currently deputy director of the key Laboratory for Smart Integrated Systems, and head of VLSI Systems Design Group. He is in charge for CoMoSy, VENGME projects for embedded systems and multimedia applications. His research interests include design and test of networks-on-chips, systems-on-chips, design-for-testability, asynchronous/synchronous VLSI design, and hardware architecture for multimedia applications. He has served as a Technical Program Committee member/ Conference Organization member for a dozen of conferences/journals including ATC 2008, ATC 2009, IEEE DELTA 2010, ATC 2010, IEEE DELTA 2011, ATC 2011, IEICE ICDV 2011, IEEE GIIS 2011, REV-JEC, and as a reviewer for many EDA conferences and journals.

He is a member of the IEEE, IEEE Circuits and Systems Society (CAS), and the Executive Board of the Radio Electronics Association of Vietnam (REV).

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